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Variation of interface trap level charge density within the bandgap of 4H-SiC with varying oxide thickness

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Abstract. Interfacial characteristics of metal oxide-silicon carbide (MOSiC) structure with different thickness of SiO_2, thermally grown in steam ambient on Si-face of 4H-SiC (0 0 0 1) substrate were investigated. Variations in interface trapped level density ($D_{\rm it}$) was systematically studied employing high-low (H-L) frequency *C–V* method. It was found that the distribution of $D_{\rm it}$ within the bandgap of 4H-SiC varied with oxide thickness. The calculated $D_{\rm it}$ value near the midgap of 4H-SiC remained almost stable for all oxide thicknesses in the range of 10^9–10^{10} cm^{-2} eV^{-1}. The $D_{\rm it}$ near the conduction band edge had been found to be of the order of 10^{11} cm^{-2} eV^{-1} for thicker oxides and for thinner oxides $D_{\rm it}$ was found to be the range of 10^{10} cm^{-2} eV^{-1}. The process had direct relevance in the fabrication of MOS-based device structures.

Keywords. 4H-SiC; wet thermal oxidation; MOSiC structure; interface trap level density.

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1. Introduction

Silicon carbide (SiC) has become one of the most recent subjects of research due to its potential capability as an electronic material for high temperature, high power, high frequency, and nonvolatile random-access-memory devices. Compared to other semiconductor materials, SiC offered unique properties like wide band-gap energy, a high value of critical electric field, high thermal conductivity and so on [1–5]. Interface properties are the most researched issue in the realization of metal oxide-silicon carbide (MOSiC) structures in the fabrication of devices. Thermal oxidation of silicon carbide surface is the most crucial process in the development of metal oxide-silicon carbide (MOSiC) based devices. However, the thermal oxide grown on SiC is found to be slightly different from

that grown on the silicon substrate and many basic oxide characterization experiments still remain to be carried out.

Recently, SiC-based MOSiC structures have been intensively investigated by many groups [6–10]. However, their expectations has not been achieved yet, because of poorer interface properties at SiO_2/SiC interface, especially in 4H-SiC [11,12]. Numerous efforts have been made to realize the variation of the interface-trapped level density near both the band edges of SiC. Some relevant works related to this issue have been carried out with a fixed silicon dioxide thickness. It seemed to examine the variation interface-trapped level density ($D_{\rm it}$) with varying oxide thicknesses within the bandgap of 4H-SiC. The evaluation of $D_{\rm it}$ is an important issue in the fabrication of MOSiC-based devices.

An experiment was conducted [13] to characterize the thermally grown SiO_2 films by *I–V* technique. Consequently, in this paper, we report systematic investigation on variation of $D_{\rm it}$ with varying oxide thicknesses in the bandgap of 4H-SiC by fabricating different oxide thickness of MOSiC structures using the wet oxidation process at 1110°C. A pictorial distribution of $D_{\rm it}$ was analysed and presented on the basis of their energy band diagram. The interface trapped level density was evaluated by means of capacitance vs. voltage (*C–V*) measurements. Experimental details of the sample preparation, fabrication of MOSiC structures and *C–V* measurement methodology are given in the next section. Acquired experimental results with discussion are mentioned in the section thereafter which is followed by conclusion.

2. Experimental details

A device grade n-type 4H-SiC substrate of 50 μm epitaxial layer on Si-face (nitrogen-doped, N concentration; 9×10^{14} cm^{-3}), 8° off-axis (0 0 0 1) oriented was used. The wafer was cut into several pieces using a special dicing blade from M/s DISCO Japan. Prior to loading in a quartz furnace for oxidation, RCA chemical cleaning treatment was given to all the samples. Samples were loaded for oxidation at 800°C with a flow of nitrogen. Wet thermal oxidation was performed at 1110°C and samples were unloaded at 800°C in nitrogen flow. This was repeated for each batch of the samples with varying oxidation time from 30 to 180 min. Oxide thickness on each sample was recorded using Ellipsometer followed by the surface profiler verification.

To fabricate the MOSiC structure, the oxide layer from the c-face or n^+ side of 4H-SiC was removed using buffer oxide etchant (BOE) by protecting the Si-face with photoresist. Ohmic contact was performed on the c-face with the deposition of composite layer of Ti (300 Å) and Au (2000 Å) using e-beam evaporation method in the vacuum range of 10^{-7} Torr. The Si-face of the oxidized 4H-SiC was retained with the grown oxide. Nickel with a thickness of 1500 Å was selectively deposited on each sample of different oxide thicknesses using e-beam evaporation in UHV. A metal mask carrying an array of 1 mm diameter was employed for the selective deposition of metal on oxide. Individual chips of MOSiC structure with varying oxide thicknesses were separated and bonded on TO-8 header using a ball-to-wedge bonder. 4284A LCR meter from M/s Agilent Technology was used for *C–V* measurement on LabVIEW platform. *C–V* characteristics were

measured under the following conditions. The measurement frequency and signal level were fixed at 1 MHz and 1 V for high frequency *C–V*, whereas 1 kHz and 1 V for low frequency. The whole measurement was performed by sweeping the DC bias from -15 V to 15 V with 0.2 V step voltage.

3. Experimental results and discussion

Figure 1 shows the typical high-frequency (H-F) *C–V* curve, measured across n-type MOSiC structures of oxide thickness variation from 17 to 65 nm. The accommodation of accumulation, depletion and inversion capacitance in the measured *C–V* curve revealed the formation of charge distribution across the structures as well as at the interface of SiO_2/4H-SiC. As the gate voltage is swept from accumulation ($+15$ V) to inversion (-15 V) or vice versa, the total gate charge can be estimated by $Q_{\rm G} = (Q_{\rm S} + Q_{\rm it})$. For the ideal case, the value of interface traps ($Q_{\rm it}$) should be zero. The relationship of the surface potential to the gate voltage having zero interface traps is known as an ideal *C–V* curve. The accommodation of charge distribution in the measured *C–V* characteristic as shown in figure 1 have all the information about the associated oxide charges within the bulk of oxide or at SiO_2/4H-SiC interface. Due to large leakage current in the oxide, most capacitors do not seem to have reached their maximum value in a strong accumulation region. The flat-band voltage continuously increases in addition to the oxide thickness in MOSiC structure. The location of the charge plays a crucial role in the determination of flat-band voltage means. When the charge is located at the SiO_2/4H-SiC interface, flat-band voltage will be maximum, because during the sweep mode all charges will contribute in the silicon carbide region. When the charge is located at the gate

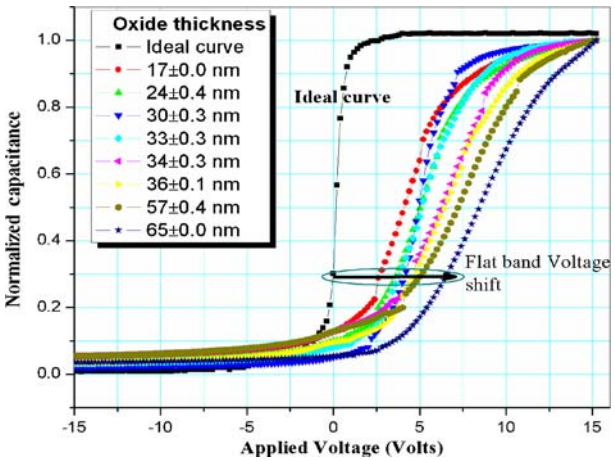

Figure 1. High-frequency *C–V* curve for different oxide thicknesses.

metal/SiO_2 interface, the effective charge will contribute in the gate oxide only and has no significant effect on the flat-band voltage. For a given charge density, the flat-band voltage reduces as the oxide capacitance increases, i.e., for thinner oxides. Hence, oxide charges usually contribute little to flat-band or threshold voltage shifts for thin-oxide MOSiC-based devices. The flat-band voltage shift from the ideal curve is caused by electrons or holes trapped at the interface states and fixed charge. To determine the various charges, one compares theoretical and experimental *C–V* curves. The acquired characteristics (figure 1) clearly indicate that the measured capacitance is biased (positive and negative) and have accumulation, depletion and inversion regions, with a significant voltage axis shift due to the presence of oxide charges. These shifts from the ideal curve provide the value of flat-band voltage. The flat-band capacitance normalized by $C_{\rm ox}$ is given by

$$\frac{C_{\rm FB}}{C_{\rm ox}} = \left(1 + \frac{136\sqrt{T/300}}{t_{\rm ox}\sqrt{N_{\rm D}}}\right)^{-1}, \tag{1}$$

where $t_{\rm ox}$ is the oxide thickness and $N_{\rm D}$ is the doping concentration.

Each *C–V* curve measured at 1 MHz for every oxide thickness has been normalized by its own oxide capacitance ($C_{\rm ox}$) and the flat-band voltage associated with the oxide thickness has been calculated with respect to shift from their ideal *C–V* curve. The variation in the flat-band voltage as a function of oxide thickness is represented in figure 1. The flat-band voltage shift for every oxide thickness is calculated and plotted as a function of oxide thickness in figure 2.

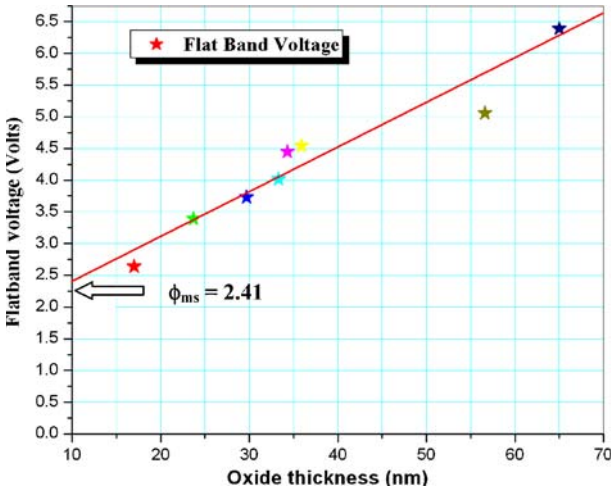

Figure 2. Flat-band voltage shift with oxide thicknesses.

These positive voltage shifts in figure 2 clearly indicate that negatively charged electrons have been injected from gate metal to oxide with the bias voltage. The distribution of fixed charge density can be computed by [14]

$$Q_{\rm fix} = (\phi_{\rm ms} - V_{\rm FB})\, C_{\rm ox}. \tag{2}$$

Here $\phi_{\rm ms}$ is the work function difference between metal and silicon carbide, $V_{\rm FB}$ is the flat-band voltage shift and $C_{\rm ox}$ is the oxide capacitance. An experimentally measured flat-band voltage shift as a function of oxide thickness has a slope $Q_{\rm fix}/C_{\rm ox}$ and an intercept of $\phi_{\rm ms}$. The measured value of $\phi_{\rm ms}$ for nickel as a gate metal and n-type 4H-SiC has been computed as 2.41 eV. The fixed charge density ($Q_{\rm fix}$) was estimated as a function of oxide thickness using eq. (2) which is summarized in table 1. In all the five samples, flat-band voltage varies from 3.4 to 6.4 V leading to $Q_{\rm fix}$ variation of -8.85×10^{11} to -1.32×10^{11} cm^{-2}. The impurity contamination during thermal oxidation process or gate material (Ni) evaporation (metallization) is supposed to be the main cause of increment in fixed charge as a function of oxide thickness.

The Terman method [15] describes the change in capacitance of a metal oxide-semiconductor (MOS) capacitor measured at a high frequency as a function of bias voltage at room temperature. The interface traps which are measured at a high frequency do not respond but do respond at low frequency with slowly varying bias voltage. The interface traps act as fixed charge and the resulting shift in high-frequency *C–V* curve gives the true evidence of interface trap density at the interface of SiO_2/SiC. On the other hand, Berglund [16] showed that interface trap density can be determined by comparing the theoretical *C–V* curve to experimental low-frequency curve because interface traps do respond at low frequency as explained above. The variation of low frequency capacitance with bias voltage is given by

$$C_{\rm LF} = \frac{1}{(1/C_{\rm ox}) + 1/(C_{\rm S} + C_{\rm it})} \tag{3}$$

where $C_{\rm S}$ is the low-frequency semiconductor capacitance and $C_{\rm ox}$ is the oxide capacitance. Interface trap density associated with $C_{\rm it}$ can be calculated by $D_{\rm it} = C_{\rm it}/q$.

$$D_{\rm it} = \frac{1}{q}\left(\frac{C_{\rm ox}C_{\rm LF}}{C_{\rm ox} - C_{\rm LF}} - C_{\rm S}\right). \tag{4}$$

Table 1. The estimated parameters of MOSiC structure for different oxide thicknesses.

Oxide thickness (nm)	$\Delta V_{\rm FB}$ (V)	$Q_{\rm fix}$ (cm^{-2})	$D_{\rm it}$ at midgap (eV^{-1} cm^{-2})	$D_{\rm it}$ at EC (eV^{-1} cm^{-2})
24±0.3	3.4±0.01	−8.84E11	2.97E9	1.29E10
36±0.1	4.6±0.01	−1.00E12	4.94E9	1.00E11
44±0.1	–	–	3.65E10	6.00E11
57±0.4	5.1±0.01	−1.01E12	6.69E10	6.10E11
65±0.0	6.4±0.01	−1.32E12	7.09E10	8.20E11

Determination of $D_{\rm it}$ at low frequency is time consuming and accuracy is not satisfactory. So a simplified standard approach is adopted to replace low-frequency measured $C_{\rm S}$ by high-frequency $C_{\rm S}$ using

$$C_{\rm S} = \frac{C_{\rm ox} C H_{\rm F}}{C_{\rm ox} - C_{\rm HF}}. \tag{5}$$

Substituting the value of $C_{\rm S}$ from eq. (5) into eq. (4), the variation of $D_{\rm it}$ in terms of the measured high- and low-frequency *C–V* curves can be computed as follows:

$$D_{\rm it} = \frac{C_{\rm ox}}{q}\left(\frac{C_{\rm LF}/C_{\rm ox}}{1 - C_{\rm LF}/C_{\rm ox}} - \frac{C_{\rm HF}/C_{\rm ox}}{1 - C_{\rm HF}/C_{\rm ox}}\right) {\rm cm}^{-2}\,{\rm eV}^{-1}. \tag{6}$$

The variation of surface potential with gate voltage for all oxide thicknesses can be estimated by

$$V_{\rm G} = \phi_{\rm S} - \phi_{\rm oxide} \tag{7}$$

whereas the voltage drop in the oxide can be calculated by

$$\phi_{\rm oxide} = \frac{\sqrt{2qN_{\rm D}K_{\rm S}\varepsilon_0\phi_{\rm S}}}{K_{\rm SiO}\varepsilon_0} X_0. \tag{8}$$

The location of the interface trap in the bandgap can be expressed as follows:

$$E_{\rm C} - E_{\rm t} = -\psi_{\rm S} + E_{\rm g}/2 + kT\ln(N_{\rm D}/n_{\rm i})q, \tag{9}$$

where $\psi_{\rm S}$ is the band-bending under certain gate bias, $E_{\rm g}$ is the energy gap of 4H-SiC, $N_{\rm D}$ is the doping concentration, $n_{\rm i}$ is the intrinsic carrier concentration of 4H-SiC, k

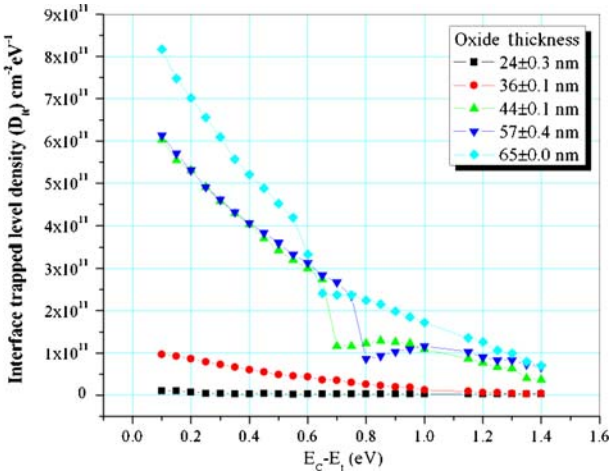

Figure 3. Distribution of $D_{\rm it}$ within the bandgap of 4H-SiC for different oxide thicknesses.

Variation of interface trap level charge density

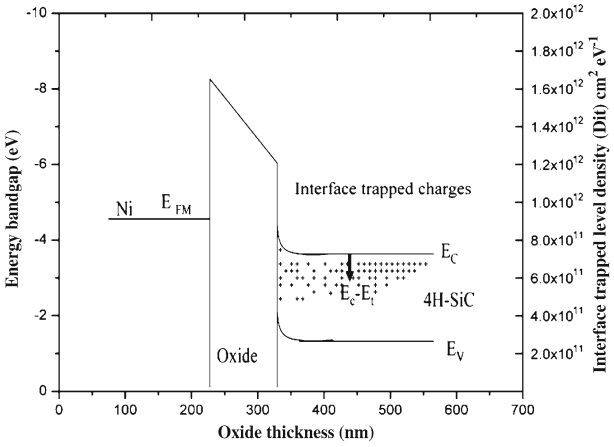

Figure 4. Pictorial diagram for MOSiC structure associated with the distribution of $D_{\rm it}$ as a function of oxide thickness.

is the Boltzmann constant and T is the absolute temperature. The value of $\psi_{\rm S}$ can be determined by comparing the measured high-frequency *C–V* curves of n-type 4H-SiC MOS capacitors with the theoretical *C–V* curve [17].

Figure 3 shows the distribution of interface trap level densities ($D_{\rm it}$) within the bandgap of 4H-SiC for the oxide thickness variation of 24$\pm$0.3 nm to 65 nm in MOSiC structures. The value of $D_{\rm it}$ was calculated using eq. (6) for the plotted oxide thickness (figure 3). The shape of the $D_{\rm it}$ distribution curve as a function of band-gap energy shows minimum value near the midgap and a sharp increment can be observed towards the conduction band ($E_{\rm C} - E_{\rm t} = 0.1$ eV) edge for thicker oxide while a very small increment for thinner oxide. The extracted $D_{\rm it}$ values near the mid-bandgap of 4H-SiC remain stable for all oxides with thicknesses in the range of 10^9–10^{10} cm^{-2} eV^{-1}. It is observed from table 1 that the fixed oxide charge density is continuously increasing with oxide thickness, which means that for a long time oxidation bulk charges of oxide (due to removal of C species during thermal oxidation [18–20]) will be more effective. The value of $D_{\rm it}$ near the conduction band edge has been found to be of the order of 10^{12} cm^{-2} eV^{-1} for thicker oxides and for thinner oxides $D_{\rm it}$ comes out in the range of 10^{10} cm^{-2} eV^{-1}. Based on our experimental results, a pictorial diagram of the interface trap level charge distribution within the bandgap of 4H-SiC is presented (figure 4) as a function of oxide thickness.

4. Conclusion

A thickness-dependent interfacial distribution of oxide charges in MOSiC structures was systematically investigated. The flat-band voltage shift of all the samples indicated positive value due to the existence of deep accepter type surface states and negative fixed charges, and these effects are highly responsible for variation in $D_{\rm it}$ with oxide thickness. The interface trap level density $D_{\rm it}$ at SiO_2/4H-SiC interface is significantly higher

near the semiconductor conduction band edge of the wet thermally oxidized epitaxial Si-face of 4H-SiC (0 0 0 1). A sharp increment in the variation of $D_{\rm it}$ as a function of oxide thickness was observed at the edge of the conduction band and near the midgap of 4H-SiC it remained constant for all oxide thicknesses.

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