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Experimental analysis of current conduction through thermally grown SiO_2 on thick epitaxial 4H-SiC employing Poole–Frenkel mechanism

SANJEEV K GUPTA[1,2,*], A AZAM[2] and J AKHTAR[1]

[1]Sensors and Nano-Technology Group, Semiconductor Devices Area, Central Electronics Engineering Research Institute (CEERI)/Council of Scientific and Industrial Research (CSIR), Pilani 333 031, India

[2]Department of Applied Physics, Z.H. College of Engineering and Technology, Aligarh Muslim University, Aligarh 202 002, India

*Corresponding author

E-mail: sanjeev@ceeri.ernet.in (Sanjeev K Gupta); azam222@rediffmail.com (A Azam); jamil@ceeri.ernet.in (J Akhtar)

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Abstract. Electrical properties of SiO_2 grown on the Si-face of the epitaxial 4H-SiC substrate by wet thermal oxidation technique have been experimentally investigated in metal oxide–silicon carbide (MOSiC) structure with varying oxide thicknesses employing Poole–Frenkel (P–F) conduction mechanism. The quality of SiO_2 with increasing thickness in MOSiC structure has been analysed on the basis of variation in multiple oxide traps due to effective P–F conduction range. Validity of Poole–Frenkel conduction is established quantitatively employing electric field and the oxide thickness using forward I–V characteristics across MOSiC structures. From P–F conduction plot ($\ln(J/E)$ vs. $E^{1/2}$), it is revealed that Poole–Frenkel conduction retains its validation after a fixed electric field range. The experimental methodology adopted is useful for the characterization of oxide films grown on 4H-SiC substrate.

Keywords. 4H-SiC; thermally grown SiO_2; metal oxide–silicon carbide structure; I–V characteristics; Poole–Frenkel conduction.

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1. Introduction

Thermal oxide reliability is one of the most critical concerns in the realization of metal oxide–silicon carbide (MOSiC) structures. Among a group of wide bandgap semiconductors, SiC competes owing to its unique capability of oxidation in the form of SiO_2 making it an obvious choice for replacing the mighty silicon MOS devices. Silicon dioxide is an extremely stable passivating layer, acts as a good electrical insulator, and forms an excellent interface with the surface of SiC. It also

serves as a very good barrier against diffusion of dopants and other impurities, and can resist a number of thermal and chemical processes. Silicon carbide is an emerging wide bandgap, compound semiconductor to fulfill its potential as an electronic material for high temperature, high power, high frequency, and nonvolatile random access memory devices. It is the most compatible material in harsh environment where silicon carbide has established its unique identity for new generation electronic devices. 4H-SiC is a polytype of SiC which has a large bandgap (3.26 eV), the highest electron mobility (800 cm^2/V-S) among hexagonal polytypes of SiC, a high value of critical electric field (3 MV/cm), high saturation velocity of electrons (2×10^7 cm/s) and high thermal conductivity (3–5 W/cm-K) [1–5]. In device fabrication, 4H-SiC has a unique impact to realize MOSiC structure-based high-power devices.

Investigation of the current–voltage characteristics seems to provide a more adequate method for distinguishing between the different mechanisms of charge transport. The mechanisms for DC conductivity at low and high electric fields in amorphous as well as crystalline materials have been discussed in the literature. Four main mechanisms have been proposed for the observed behaviour: direct tunnelling (DT), Schottky emission (SE), Fowler–Nordheim (FN) tunnelling and Poole–Frenkel (P–F) conduction, depending upon the magnitude of oxide thickness, defect at the interface and polarity of the applied gate voltage [6–8]. P–F conduction mechanism is most often observed in amorphous materials, particularly dielectrics, because of the relatively large number of defect centres present in the energy gap. In fact, the particular host material, where the defects reside, can basically be viewed as acting only as a medium for localized defect states. The P–F conduction effect has been observed in many dielectric materials which are commonly used in 4H-SiC-based microelectronic device fabrication. For example, nitrided SiO_2 [9], HfO_2/nitrided SiO_2 [10], HfO_2 [11], Al_2O_3 [12], and so on which hold great potential as the gate oxide, have shown that current conduction in these materials is bulk-limited which is governed by the P–F conduction. Currently, one of the most important dielectric material used in microelectronics is SiO_2, which can be easily grown thermally on SiC substrate in steam as well as dry ambient.

In this paper, we report systematic investigation of current conduction mechanism produced by Poole–Frenkel conduction across MOSiC structure with varying oxide thicknesses on device-grade epitaxial 4H-SiC substrate. Wet thermal oxidation technique has been used to grow SiO_2 at a fixed temperature of 1110°C for different oxidation time. Experimental details of sample preparation, fabrication of MOSiC structures and I–V measurement methodology are given in the next section. Experimental results and discussion are given in the section thereafter which is followed by conclusions.

2. Experimental details

A device-grade n-type 4H-SiC substrate of 50 μm epitaxial layer on Si-face (nitrogen-doped, N_2 concentration: 9×10^{14} cm^{-3}), 8° off-axis (0 0 0 1) orientation was used. The wafer has been cut into several pieces using the special dicing blade from M/s DISCO Japan. Prior to loading in a quartz furnace for the oxidation, RCA chemical cleaning treatment was given to all the samples. Samples

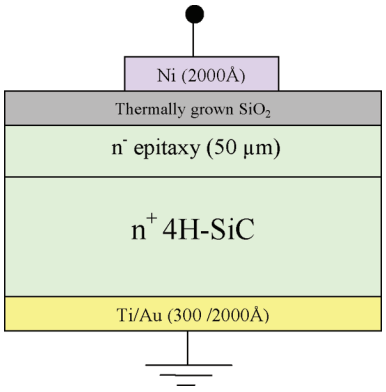

Figure 1. Schematic of metal oxide-silicon carbide (MOSiC) structure.

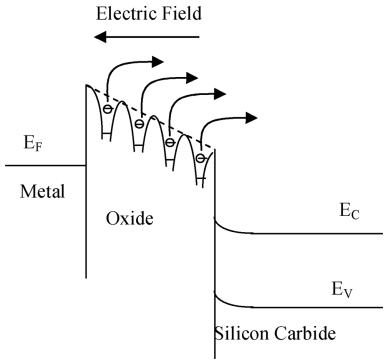

Figure 2. Energy band diagram for Poole–Frenkel conduction in MOSiC structure having multiple Coulombic traps.

were loaded for oxidation at 800°C in nitrogen atmosphere. Wet thermal oxidation has been performed at 1110°C and samples were unloaded at 800°C in nitrogen flow. This was repeated for each batch of samples with varying oxidation time from 30 min to 180 min. Oxide thickness on each sample was recorded using the ellipsometer followed by a surface profiler verification. In order to fabricate the MOSiC structure, oxide layer from the c-face of 4H-SiC was removed using buffer oxide etchant (BOE) by protecting the Si-face with photoresist. Ohmic contact was performed on c-face with the deposition of a composite layer of Ti (300 Å) and Au (2000 Å) using e-beam evaporation method in the vacuum range of 10^{-7} Torr. The Si-face of the oxidized 4H-SiC was retained with the grown oxide. Nickel (2000 Å) as gate metal was selectively deposited through a metal mask carrying array of 1 mm diameter using e-beam evaporation in UHV. Figure 1 shows the schematic diagram of fabricated MOSiC structure. A metal mask carrying array of 1 mm diameter was employed for the selective deposition of metal on oxide. Individual chips of MOSiC structure with varying oxide thicknesses were separated and bonded on TO-8 header using ball-to-wedge bonder. HP 4140B pA meter/DC voltage source was used for I–V measurement on LabVIEW platform. The whole measurement was performed by sweeping the DC bias from 0 to 5 V with 0.1 V step voltage.

3. Experimental results and discussion

Many current conduction phenomena occur when insulating films are sandwiched between two electrodes. The identification of the dominant current conduction mechanism is important to understand the current–voltage characteristics of the structure being studied. There are two broad categories to describe these mechanisms: electrode-limited and bulk-limited. Electrode-limited or barrier-limited mechanisms operate in the vicinity of the interface between the insulator and the contacts. The transport of charge carrier into the insulator limits the current

conduction. Schottky emission and Fowler–Nordheim tunnelling are the most prominent examples of these types of mechanisms. In the bulk-limited case, the current is limited by the transport of carriers through the insulator. In other words, sufficient number of carriers are injected into the insulator, but they experience difficulty in reaching the other electrode due to bulk transport limitations. Examples are intrinsic and Poole–Frenkel conduction mechanisms. Current conduction mechanisms through gate dielectric in 4H-SiC-based MOSiC structures have been well explained by Cheong *et al* [10]. Figure 2 shows the P–F conduction in MOSiC structure that is basically a parallel plate capacitor. This diagram is fundamental to the effect in any MOSiC device. The dashed line indicates the quasi-conduction band of the oxide in the absence of any traps. When an electric field is applied as shown, the trapped electrons can enter the oxide's quasi-conduction band by the Poole–Frenkel mechanism and flow from the oxide across the SiC/SiO_2 interface into the silicon carbide conduction band edge. The Poole–Frenkel effect can be observed at high electric field. The standard quantitative equation for P–F conduction is

$$J_{\mathrm{PF}} = E \exp\left[\frac{-q(\phi_{\mathrm{B}} - \sqrt{qE/\pi\varepsilon_i})}{kT}\right], \tag{1}$$

where J_{PF} is the current density due to Poole–Frenkel conduction, T is the absolute temperature, q is the electronic charge, ϕ_{B} is the potential barrier at the metal and insulator interface, E is the electric field in the insulator, ε_i is the dielectric constant and k is the Boltzmann constant. Current conduction through different thickness of silicon dioxide of an n-type 4H-SiC-based metal oxide silicon carbide structure as discussed above, and with the gate voltage varying between 0 and 5 V, was measured at room temperature. The lifetime of a particular gate oxide thickness is determined by the total amount of charge carriers that flow through the gate oxide under the influence of electric field. Ideally, an oxide layer does not allow charge carrier to pass through. It has been previously reported that for an oxide with thickness between 5 and 50 nm, the current conduction is explained by Fowler–Nordheim tunnelling and for an oxide with thickness greater 50 nm the current conduction is explained by Schottky emission [7]. If the oxide thickness is greater than 50 nm, having some trapped charge inside it, it can be governed by Poole–Frenkel conduction model. On the other hand, current conduction for the ultrathin oxide layers less than 5 nm, has been termed as direct tunnelling [8]. Figure 3 shows the current–voltage characteristics across MOSiC structure for different gate oxide thicknesses starting from 23.7 nm to 61.4 nm. This plot revealed that resistance of the bulk material increases with oxide thickness and it provides the knowledge of bulk limited current conduction mechanism through insulator.

Poole–Frenkel conduction results from field-enhanced excitation of trapped charge into the conduction band of insulator indicate the presence of electron traps in the case of thick insulating layer. At room temperature the traps do not donate electrons, i.e. free electron, to the conduction band of silicon carbide or accept electron from valence band, i.e. free holes, because they are located many $k_{\mathrm{B}}T$ below the conduction band (for donors) and above the valence band (for acceptors). One possible reason for this is the fact that the applied electric field E is simply assumed to be equal to V/d where V is the applied voltage and d is the physical thickness of the sample. The functional dependence of conductivity on electric field

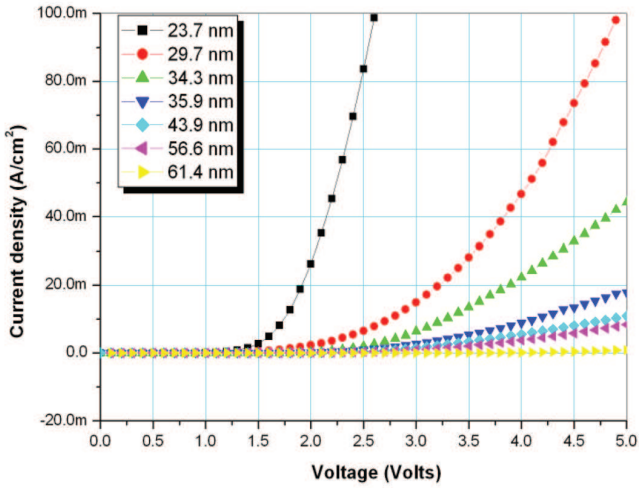

Figure 3. Current conduction through different thicknesses of SiO_2 across MOSiC structure in strong accumulation condition.

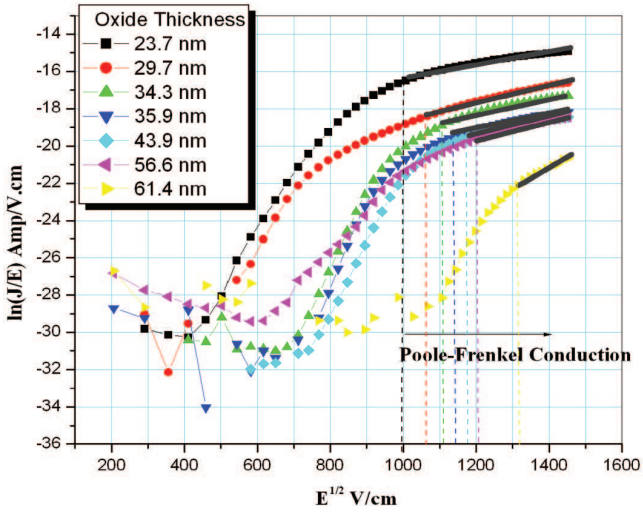

Figure 4. Plot of $\ln(J/E)$ vs. $E^{1/2}$ showing P–F conduction range for different thicknesses of SiO_2 in MOSiC structure.

strength in different thicknesses of SiO_2 in MOSiC structure can be differentiated from their different rates of change of conductivity with electric field strength by a plot of $\ln(J/E)$ vs. $E^{1/2}$, and is shown as a straight line in figure 4. At fields greater than 9.910×10^5 V/cm for 23.7 nm oxide thickness, electrons in the SiO_2 bulk traps gain sufficient energy to be excited to the conduction band of silicon carbide and Poole–Frenkel conduction becomes the dominating conduction mechanism beyond that electric field. Similarly, the applied electric field greater than 1.128×10^6

V/cm for 29.7 nm oxide thickness, 1.232×10^6 V/cm for 34.3 nm oxide thickness, 1.301×10^6 V/cm for 35.9 nm oxide thickness, 1.385×10^6 V/cm for 43.9 nm oxide thickness, 1.458×10^6 for 56.6 nm oxide thickness and 1.755×10^6 V/cm for 61.4 nm oxide thickness shows a typical linear plot of dominating Poole–Frenkel conduction mechanism in thermally grown SiO_2 on thick epitaxial 4H-SiC substrate.

4. Conclusions

A systematic experimental study of electrical transport governed by Poole–Frenkel conduction mechanism in MOSiC system with varying oxide thicknesses has been presented. For the oxide thickness variation from 23.7 nm to 61.4 nm, the subsequent electric field responsible for the start of P–F mechanism varies from 9.9×10^5 V/cm to 1.7×10^6 V/cm. From the P–F plot it is revealed that the electric field limit for the onset of P–F mechanism shifts to higher electric field with increasing oxide thickness. A deep level trap realization is suggested with increasing oxide thickness.

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