Development Of Polycrystalline Diffused Piezoresistors Using E-Beam Evaporation Method For MEMS Applications

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Abstract

This paper describes an alternate experimental technique to deposit the polycrystalline silicon (Poly-Si) thin film for the fabrication of diffused piezoresistors. In this process the deposition of poly-Si film (2000Å) was carried out using e-Beam evaporation metho high vacuum with controlled deposition rate on the bed of oxidized p-type Si <100> wafers. The grain size of Poly-Si was analyzed using Scanning Electron Microscopy (SEM), which is found to be around 45 to 50 nm. The thermal doping of boron was performed at different temperature for fixed time in a horizontal quartz furnace. The sheet resistance of all samples was measured using four probe techniques. The sheet resistance of deposited film decreases continuously with doping temperature, which itself describes like the conventional polysilicon nature. The diffused piezoresistors were fabricated and their measured values are analyzed and reported in this paper. The developed experimental process provides a sufficient yield, low cost and highly repeatability in the realization of polysilicon film while developed technology for diffused resistors is useful in the fabrication of electronic sensor, gate metal in CMOS process and so on.

Keywords : Polysilicon, e-beam evaporation, SEM, doping, MEMS

1. Introduction

Polysilicon is the most extensively used structural material in surface micromachining due to its good mechanical properties and well-established processing technology for a variety of applications such as in the fabrication of pressure sensors, micro-switches, cantilevers, suspended structure, rotors etc [1-3]. In the fabrication of above described elements or structures polysilicon serve as a structure material and silicon dioxide or silicon nitride as the sacrificial spacer layer. The performance and control of the dimensions of these elements are extensively dependent on the residual stress, and stress gradient in the structural layer.

Piezoresistive property of the polysilicon film, along with its high-temperature stability, is accountable for its emerging potentials in the MEMS based device applications. In general routine the electrical conductivity of the films has been adjusted using doping process with

suitable dopants either by thermal doping or ion implantation methods. However, doping distribution of the species in case of polysilicon does not follow the same way as it is characterized in single-crystalline silicon. Effect of grain boundaries on the doping distribution in the polysilicon layers has been studied with findings related to doping species confining to the edges of the grains [4]. Owing to its increasing applications, efforts are being made to characterize the Poly-Si films particularly deposited on insulating bed using LPCVD techniques [5].

Silicon dioxide thin film has a compressive internal stress, less stiff than other thin film materials, has unique electrical properties are frequently used as a mechanical material in high sensitivity applications. On the other hand, silicon dioxide, with its low thermal conductivity, is a natural thermal insulator, which has been exploited for the production of integrated thermal detector. In MEMS technology, it is used to electrically isolate components and has been used in some recent applications as a structural material [6].

Low pressure chemical vapour deposition (LPCVD) is a standard technique to deposit the polysilicon for microelectronics processes. It has found wide acceptability and is being extensively used for surface micromachining applications also particularly in the area of MEMS technology. LPCVD polysilicon is obtained by pyrolytic decomposition of silane (SiH_4) at low pressure in the temperature range of $550–700^{0}$C. It is well known that the deposition parameters such as temperature, pressure, and flow rate have a profound effect on the structure and properties of the deposited polysilicon film. Since the above described process depends upon many parameters, therefore number of problems, however, which arise from the increasing use of hazard gases during LPCVD process like non uniformity in the yield, non repeatability and high process cost [7, 8]. To overcome these problems, an experimental method has been suggested and reported here to deposit the polysilicon film by some alternate technique, which provides a sufficient yield, low cost and highly repeatability.

A lot of works have been developed world wide using polysilicon thin films for MEMS application. Very limited research groups are working on alternate poly-Si resistors for such type of MEMS application [9, 10].

In this paper, Poly-Si film has been realized on the bed of silicon dioxide over p-type silicon (100) substrate using e-beam evaporation method in high vacuum with constant deposition rate. The deposited Poly-Si film was doped using thermal diffusion of boron at three different temperatures to adjust the desired sheet resistivity. The grain size of the Poly-Si film has been analyzed using Scanning Electron Microscopy (SEM). The developed process is likely to be the replacement of LPCVD polysilicon film with improved qualities. The details of the experiment carried out are presented in the next section. The obtained results with sufficient discussion were presented in section thereafter which is followed by conclusions.

2. Experimental Details

A p-type silicon substrate of 2'□diameter and <100> oriented was used in this experiment. The resistivity of the wafer was 1-10 Ω-cm and the thickness of wafer was about

325 to 375µm. Prior to load the samples for thermal oxidation, through chemical cleaning treatments were given to all samples as follows:

Degreasing: There are three incessant steps involved in this cleaning method (a) dip the wafer in 1,1,1-trichloroethane (TCE), and boil for 10 minutes (b) dip the wafer in Acetone, boil for 10 minutes and then (C) dip the wafer in Methanol, boils for 10 minutes. This is followed by rinse the wafer in De-ionized water.

Piranha: The solution contains H_2SO_4: H_2O_2 in the ratio 7:1.Samples ware immersed in solution for 10 minutes followed by thoroughly rinse in DI water. In next step, samples were immersed in HF solution (2%) for very short time to make surface hydrophobic [11].

Samples were loaded for oxidation at 800ºC with a flow of nitrogen atmosphere. A well optimized dry-wet-dry oxidation process was adopted [12]. Initial dry oxidation was performed for 10 minutes to realize the better contacts or interface. Now, the wet thermal oxidation was performed at 1100ºC for 2 hrs. Finally, again dry oxidation was performed for 10 minutes. All wafers were unloaded at 800ºC in nitrogen flow. Oxide thickness of the samples was recorded using ellipsometer followed by surface profiler verification. Thickness of SiO_2 layer has been found of 0.5 micron. The deposition of polysilicon was carried out in Varian's e-Beam evaporation unit in ultra high vacuum. During the evaporation, the vacuum chamber of the order of 10^{-7} torr was maintained using vac-ion pump and Ti-sublimation pump. The deposition rate of polysilicon was controlled by varying the filament current of e-gun. The total thickness of polysilicon was estimated to be 2000 Å in 27 minutes of deposition.

In order to fabricate piezoresistors, the deposited polysilicon film was thermally diffused at different temperature. Since, four wafers were used to conduct the experiment so each was diffused at different temperature. Boron thermal doping was carried out in a horizontal quartz furnace at three different temperatures of 950°C, 1000°C and 1050°C, for constant 40 min. The sheet resistance of all samples was measured using four probe techniques. The piezoresistors having length of 400µm and width of 10 µm were delineated using Optical photolithography. The unwanted polysilicon was etched out in electronic grad poly-etchant. The contact metal lines were delineated by the deposition of a composite layer of Ti (3000 Å) and Au (2000Å) using e-beam evaporation technique in the vacuum range of 10^{-7}torr. The details of the process flow are as follows (fig.1). Figure 2 (a) shows the optical image of fabricated diffused piezoresistors having contact pads and (b) shows the optical image of a single diffused resistor prior to delineate the metal contact lines.

3. Experimental Results and Discussions

A. Analysis of grain size

To analyze the grain size of deposited polysilicon film, SEM m/s Jeol, model JSM- 6390 LV was employed. In this method a high energy electron beam was produced by thermal emission source, such as a heated tungsten filament, or by a field emission cathode. The electrons are focused into a sample beam by a series of electromagnetic lenses in the SEM column. The electron beam is scanned in a raster pattern over the surface of imaging. The incident electrons cause electrons to be emitted from the sample due to elastic and inelastic scattering events

within the sample's surface or near-surface material. Emitted lower energy electrons resulting from inelastic scattering are called secondary electrons. Using this mode a high resolution imaging of deposited Poly-Si was observed as shown in figure 3 (a). Figure 3(b) shows the grain size distribution at large magnification, which comes to be 45-50 nm over the entire surface.

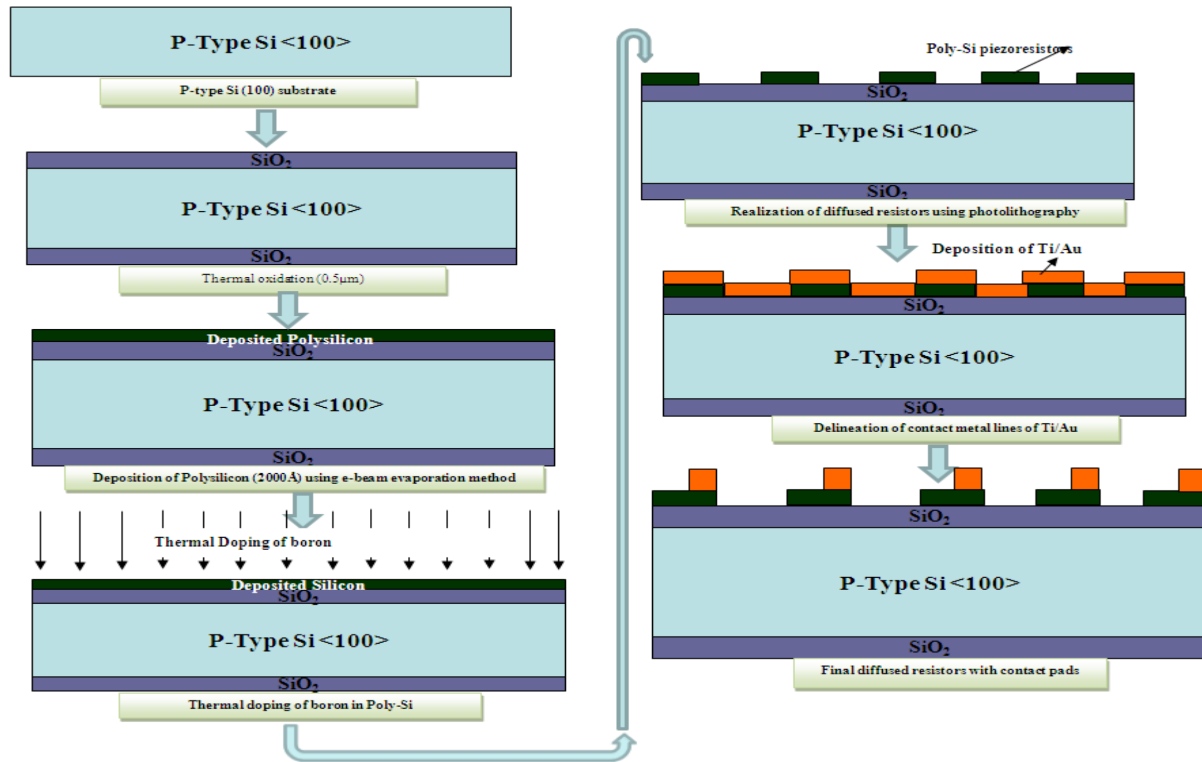

Fig. 1: Schematic Flow for the Fabrication of Diffused Polysilicon Resistors

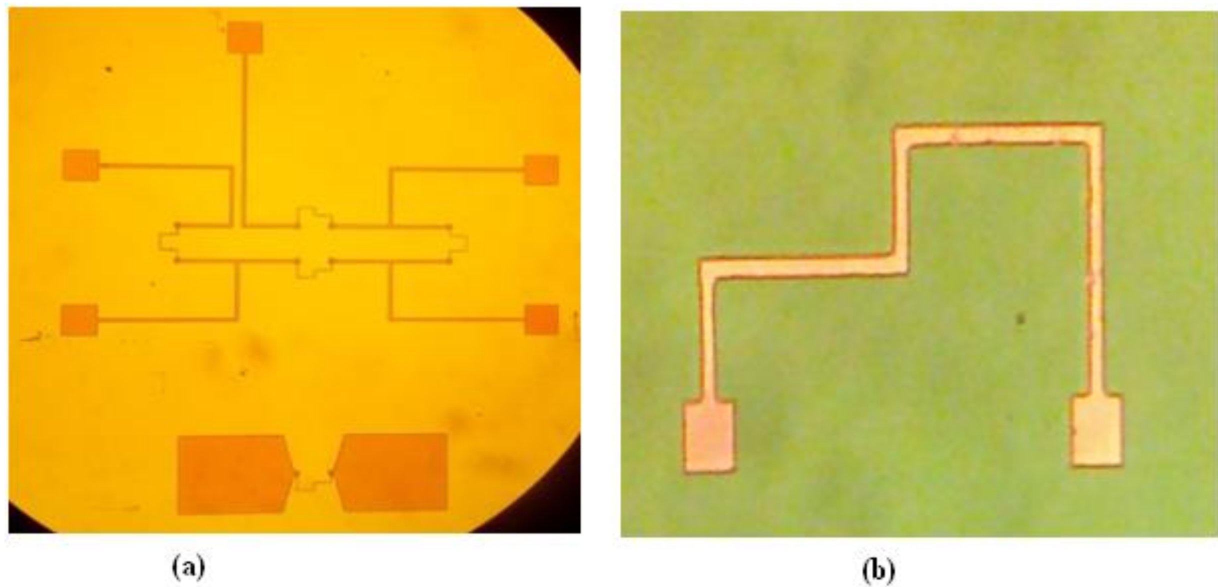

Fig. 2: (a) Optical image of fabricated diffused resistors with contact metal lines (Ti/Au) and (b) delineation of resistors prior to metal pad contact.

4. Experimental Results and Discussions

4.1 Analysis of grain size

To analyze the grain size of deposited polysilicon film, SEM m/s Jeol, model JSM-6390 LV was employed. In this method a high energy electron beam was produced by thermal emission source, such as a heated tungsten filament, or by a field emission cathode. The electrons are focused into a sample beam by a series of electromagnetic lenses in the SEM column. The electron beam is scanned in a raster pattern over the surface of imaging. The incident electrons cause electrons to be emitted from the sample due to elastic and inelastic scattering events within the sample's surface or near-surface material. Emitted lower energy electrons resulting from inelastic scattering are called secondary electrons. Using this mode a high resolution imaging of deposited Poly-Si was observed as shown in figure 3 (a). Figure 3(b) shows the grain size distribution at large magnification, which comes to be 45-50 nm over the entire surface.

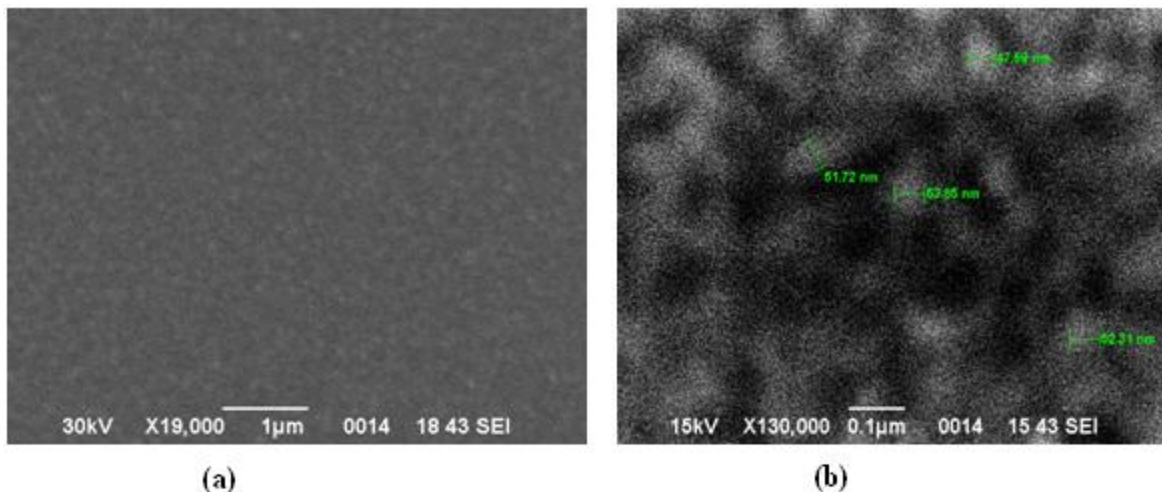

Figure 3: SEM image of polysilicon film.

4.2 Analysis of Boron Diffusion in Polysilicon Film

The piezoresistive effects are one of the most important factors in the fabrication of sensors based on MEMS technology. Basically, piezoresistive materials are placed on the top of moving membrane. The thickness of diaphragm can be controlled with optimized bulk micromachining etching process. There are many dopants have been tried to make polysilicon piezoresistive. Thermal doping of boron and phosphorus are most dominating dopants. The boron atom is smaller than silicon, and germanium is larger, which prevents stresses from volume mismatch building up. Germanium is a column-IV element beneath silicon and therefore isoelectronic with silicon, so no electrical effects are introduced.

In this experiment thermal doping of boron at different temperature was performed in deposited polysilicon. Concentration dependent diffusion flux can be described by Fick's first law:

$$j = -D(\partial N/\partial X) \qquad \text{...............(1)}$$

Where D is the diffusion coefficient (cm^2/s), N is concentration (in cm^{-3}). Diffusion coefficients can be presented by:

$$D = D_0 e^{(-E_a/KT)} \quad \text{……………..(2)}$$

Where D_0 is the frequency factor, E_a is the activation energy, K is the Boltzman's constant, K = 1.38×10^{-23} J/K and T is the temperature in Kelvin.

The sheet resistance of doped layers can be estimated by:

$$1/R_S = q\mu X_j\, N(X) \quad \text{…………… (3)}$$

Where, q is the elementary charge, μ is the mobility, N(x) is the dopant concentration and x_j is the depth from polysilicon surface.

Experimentally, the sheet resistances of all doped polysilicon were measured using four probe method. The sheet resistance of the doped films ranged from 8500 Ω/□ for a 950°C/30 minutes diffusion to 550 Ω/□ for a 1050°C/30 minutes diffusion. It is well known that grain growth in polysilicon is principally controlled by grain boundary migration which, in turn, is influenced by many factors. As doping temperature increases the segregation to the grain boundaries can reduce grain boundary mobility by pinning them. In case of polysilicon doped with arsenic or phosphorus since they segregate in extensive quantities to the grain boundaries, but since little or no segregation of boron to the grain boundaries has been suggested, little pinning of the grain boundaries should occur in polysilicon heavily doped with boron dopants. Also, it is well established that the presence of large concentrations of dopants such as boron, phosphorus, or arsenic enhances their diffusivities in polysilicon, increasing grain boundary mobility. At the polysilicon surface, doping concentration was calculated using equation 3. In this experiment depths from poly-Si surface towards the bulk was varied manually and other known parameters were putted as it. Doping concentration was found in the range of 8×10^{20}, 9×10^{19} and 1.25×10^{19} for the wafer doped at 1050°C, 1000°C and 950°C respectively. It has been also observed that these doping concentration decreases exponentially with depth towards bulk of the polysilicon as shown in figure 4. Since, at high doping temperature, the grain boundary mobilities increases due to high doping concentration, as the result of this mechanism sheet resistance of polysilicon film decreases with increasing doping temperature as shown in figure 5.

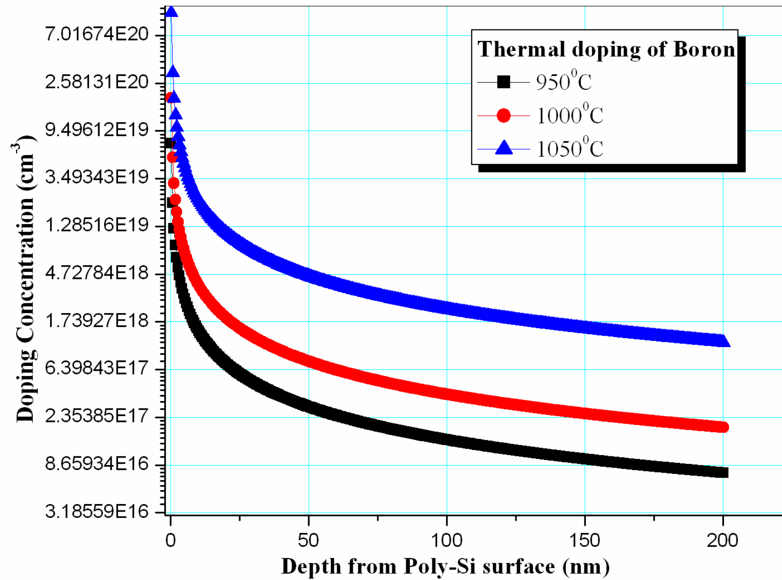

Fig.4: Variation of Doping Concentration From Poly-Si Surface Towards the Bulk at Different Temperatures

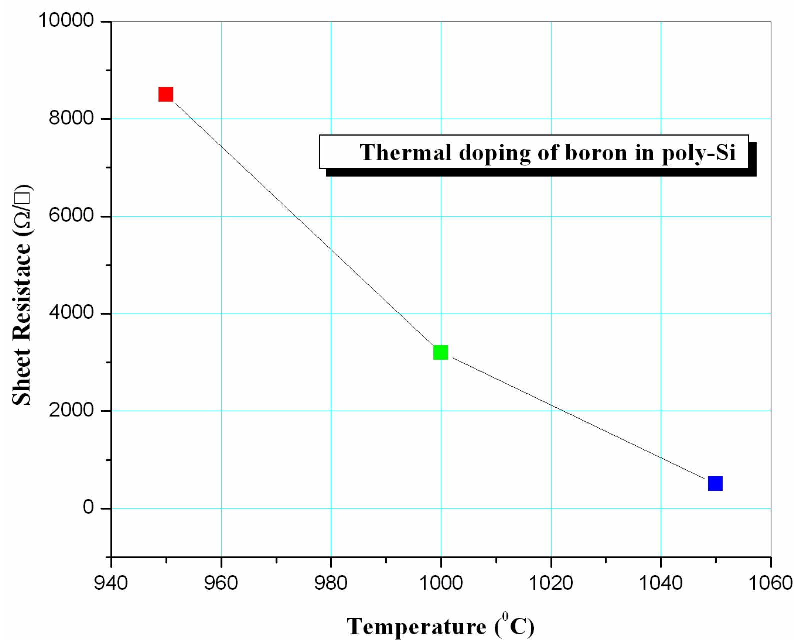

Fig 5: Measured Sheet Resistance for Different Doping Temperatures

4.3 Analysis of measured resistance

The details of the realization of diffused polysilicon resistors are described in experimental section of this paper. Figure 6 (a) shows the fully processed p-type silicon wafer surface carrying polysilicon resistors in Whetstone's bridge configuration on the oxidized surface. A uniform shape and size of piezoresistors were observed throughout the wafer using optical microscope. There are no undercut or over etched resistors were found in the layout of the silicon resistor. At the some places (near edge of the wafer) resistor width is decreased because the condensational etching of polysilicon starts from edges. The width of the resistors

is etched out completely at some of the locations on the wafer surface, which leads to infinite values of the fabricated resistors. The over etching of silicon resistors on the oxidized silicon wafer is accounted maximally for the reduced yield in the fabrication of sensor chips. A reproducible method for realizing uniform silicon resistors is a crucial requirement for a sensor foundry with high sensitivity. The experiment carried out in this report introduces a viable and cheaper technique to provide uniform and reproductive polysilicon resistors in the fabrication of micro sensors at large-scale for sensor foundry.

A 2' diameter oxidized p type silicon wafers carrying chips in 9×9 matrix have been characterized on wafer level. The resistor's values were measured using commercial probe system with attached In house developed Lab VIEW based programmable instruments. The value of resistance was recorded using Agilent 4284A LCR meter. The values of resistors were found in the range of 500-700 kΩ for the wafer, which was doped at 950^0C as shown in figure 6 (b). The distributions of resistors are quite satisfactory on whole wafer. The process has been extremely useful in the fabrication of Piezoresistive pressure sensors based on bulk micromachining using polysilicon deposited by e-beam method. The over etched width of the polysilicon resistors increases the resistor's value near the edge of the wafer, as shown in figure 6 (b).

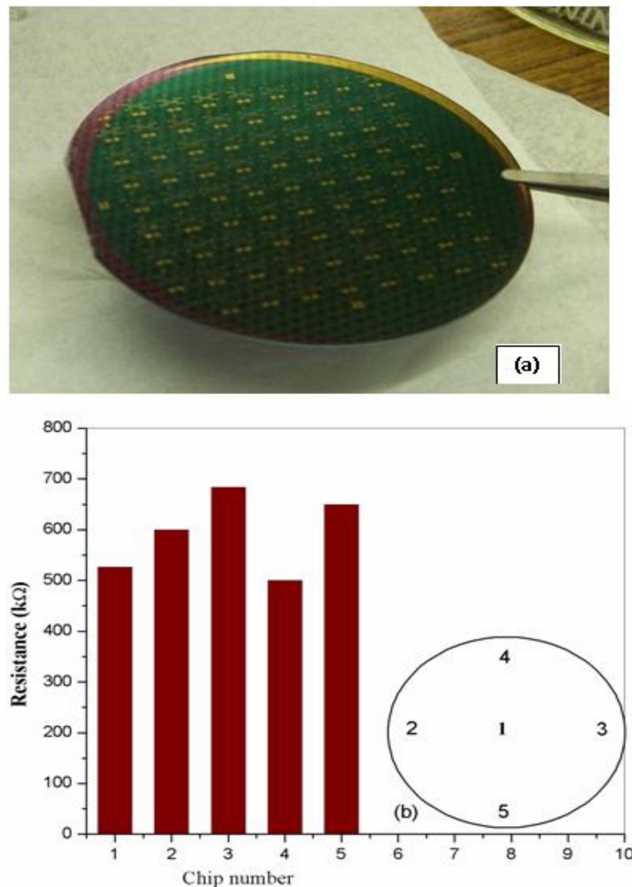

Fig. 6: Piezoresistors values of some selected chips. (a) Shows the fully processed wafer and (b) shows the location of chips, where the value of piezoresistors were measured.

5. Conclusions

In this paper an alternate experimental method has been reported to deposit the polysilicon film, which provides a sufficient yield, low cost and highly repeatability. The developed process for deposition of Polysilicon using e-beam evaporation is likely to be the replacement of LPCVD polysilicon. The following conclusion has been drawn from the above experimental study:

a) Deposited polysilicon have the grain size of 45 to 50 nm, which was calculated using SEM.
b) Sheet resistance of the films decreases linearly with thermal diffusion temperature.
c) Diffused polysilicon resistors were fabricated and their values were reported in this paper.
d) The film deposited by e-beam evaporation method can easily be used as sacrificial layer in the fabrication of electronic sensors, gate metal in CMOS process technology and so on.

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