Experimental analysis of I-V and C-V characteristics of Ni/SiO_2/4H-SiC system with varying oxide thickness

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Abstract

Purpose – The purpose of this paper is to electrically examine the quality of thin thermally grown SiO_2 with thickness variation, on Si-face of 4H-SiC $<0001>$ (having 50 μm epitaxial layer) by current-voltage (I-V) and capacitance-voltage (C-V) methods.

Design/methodology/approach – Metal-oxide-silicon carbide (MOSiC) structures with varying oxide thickness have been fabricated on device grade 4H-SiC substrate. Ni has been used for gate metal on thermally oxidized Si-face and a composite layer of Ti-Au has been used for Ohmic contact on the highly doped C-face of the substrate. Each structure was diced and bonded on a TO-8 header with a suitable wire bonding for further testing using in-house developed LabVIEW-based computer aided measurement setup.

Findings – The leakage current of fabricated structures shows an asymmetric behavior with the polarity of gate bias (+ V or − V at the anode). A strong relation of oxide thickness and temperature on effective barrier height at SiO_2/4H-SiC interface as well as on oxide charges have been established and reported in this paper.

Originality/value – The paper focuses on the development of 4H-SiC based device technology in the fabrication of MOSiC-based integrated structures.

Keywords Semiconductor technology, Silicon

Paper type Research paper

1. Introduction

Silicon carbide (SiC) is an interesting semiconductor material for electronic devices and sensors to work under harsh environment and high temperatures. The number of published research articles devoted to SiC in every year (Raynauld, 2001) clearly indicate that a continuous progress is being carried out to develop SiC technology at par with silicon and GaAs technologies (Akhtar *et al.*, 2007) by utilizing its unique properties; wider band gap, higher thermal conductivity, higher saturation velocity for electron and higher break down electric field and so on. Among the group of wide band gap semiconductors, SiC competes owing to its unique capability of oxidation in the form of stable SiO_2 (the insulating material most studied and frequently used in semiconductor technology), making it an obvious choice for the replacement of silicon metal-oxide-semiconductor (MOS) devices with excellent characteristics. SiO_2 as insulating layers in the MOS technology plays many important utilities such as a mask layer in doping processes, passivation of semiconductor surface, electrical insulation of the active area of the semiconductor device and shielding the device from environmental exposures. On the other hand, thin thermally grown films are widely used as gate dielectrics in MOS field-effect transistor structures, as insulating layers in multilevel interconnects, as capacitor dielectrics in dynamic random access memory, in thin film transistors or for solar energy devices. The basic requirements on these films are

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high breakdown field strength, low leakage currents, high resistance, and low oxide defect density that is why a rigorous study is needed in order to develop a better quality of SiO_2 on SiC substrate.

The metal-insulator-silicon carbide (MOSiC) structures consist of a silicon carbide substrate covered by an insulator layer (such as HfO_2, SiO_2, or other insulating materials), sandwiched between two metal electrodes. These structures could be fabricated either with thin dielectric layer ($t_{diel} < 5$ nm) or thick dielectric layer ($t_{diel} > 5$ nm). These structures behave like a parallel plate a capacitor, which stores the electric charge by virtue of the dielectric property of insulator or oxide layers. Owing to its importance in SiC technology, the oxide/SiC (such as SiO_2/SiC, HfO_2/SiC, TiO_2/SiC and so on) interface and associated defects on its vicinity have been extensively studied in the past some years. The basic principle of reducing the MOS scaling indicate that when we reduce the lateral dimension of MOS devices, the vertical dimension must be modified according to the device dimension. A variety of other materials like HfO_2 (Wolborski *et al.*, 2007), TiO_2 (Coleman *et al.*, 2007), Ta_2Si (Perez-Tomas *et al.*, 2005), Al_2O_3 (Avice *et al.*, 2006; Cheong *et al.*, 2007; Paskaleva *et al.*, 2005) double layer of Si_3N_4/SiO_2 (Berberich *et al.*, 2000) and so on have been intensively attempted in SiC-based MOS scaling technology. Current conduction through gate oxide might affect the performance of devices that employ the MOSiC structure, and it can be dominating factor in device down scaling (Ranuarez *et al.*, 2006). High quality thin SiO_2 is most demanded gate oxide from the semiconductor industries to reduce the cast and process steps in the device fabrication. A various oxidation process has been adopted such that dry oxidation (Vickridge *et al.*, 2007), wet oxidation (Yano *et al.*, 1999), chemical vapour deposition (CVD) (Kamimura *et al.*, 2001), and pyrogenic oxidation (Lai *et al.*, 2004; Meakawa *et al.*, 2005; Zetterling *et al.*, 1998) in order to achieve the most suitable process to realize the SiC-based MOSiC structures. Numerous studies (Eckhard *et al.*, 2005; Mark *et al.*, 2006; Chen *et al.*, 2008) shows the presence of C species in the thermally grown oxide directly affect the interface as well as dielectric properties MOS structures (Vathulya *et al.*, 1998). For this reason, rigorous studies on electrical behavior of thermally grown SiO_2 on SiC play a fundamental role in the understanding and control of electrical characteristics of SiC-based devices.

Current conduction mechanism and surface states density of MOSiC structures are important parameters that affect their main electrical parameters. When a voltage is applied across MOSiC structures, the combination of interfacial oxide, depletion, accumulation, and inversion layers of devices will share the applied voltage. Current voltage (I-V) and capacitance voltage (C-V) measurement is the key techniques to determine the quality of any insulating layer in MOS structures. The current transport mechanism from gate metal through the insulator to semiconductor could be well examined by well-established conduction models. A precise knowledge of current conduction through thermally grown SiO_2 has a unique impact to realize a high power, high temperature, high breakdown, MOSiC structure-based devices. At large electric fields and temperature, the existing charge carrier may tunnel through the forbidden region to allowed state of the insulator by field emission across the insulator. Capacitance-voltage (C-V) measurement technique is one of the most eminent tools to extract the bulk properties of SiO_2 as well as SiO_2/4H-SiC interface properties.

In Si-based MOS system, charge transport mechanisms in oxide are strongly dependent on the oxide thickness, while flatband voltage (V_{FB}) and interface trap density are not (Itsumi, 2002; Dumin, 2002). Therefore, the assumption used in SiC-SiO_2 system is questionable, and it is extremely important to investigate the dependency of oxide thickness on quality of oxide in detailed. In this paper, the quality of thin thermally grown SiO_2 with thickness variation, on Si-face of 4H-SiC $<0001>$ (having 50 μm epitaxial layer) has been electrically examined by current-voltage (I-V) and capacitance-voltage (C-V) methods. Wet thermal oxidation technique has been used to grow SiO_2 at the fixed temperature of 1,110°C for different oxidation time. Experimental details of sample preparation, fabrication of MOSiC structures and electrical characterization methodology is given in the next section. Current conduction mechanisms, extraction of different MOSiC parameters acquired results with discussion are mentioned in the section thereafter, which is followed by conclusions.

2. Experimental details

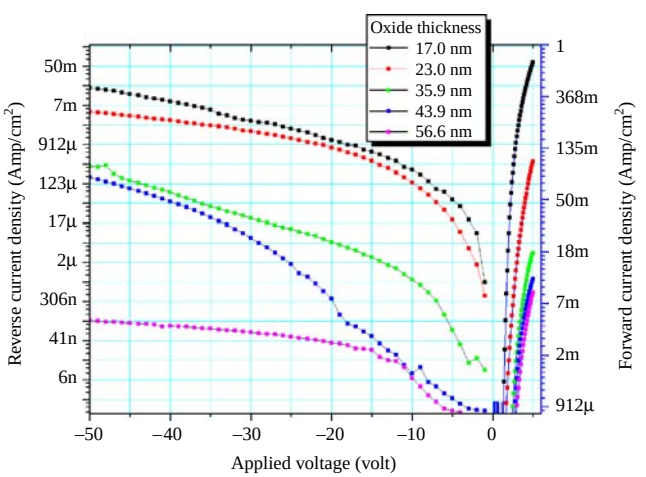
A device grade $n/n^+ -$ type 4H-SiC substrate of 50 μm epitaxial layer on Si-face (nitrogen doped, N concentration; 9×10^{14} cm^{-3}), 8° off axis (0001) oriented was used. The wafer has been cut into several pieces using a special dicing blade from M/s DISCO Japan (Akhtar *et al.*, 2007). Prior to loading in a quartz furnace for the oxidation, radio corporation of America chemical cleaning treatment was given to all the samples. Samples were loaded for oxidation at 800°C with a flow of nitrogen. Wet thermal oxidation has been performed at 1,110°C for 3 h and samples were unloaded at 800°C in nitrogen flow. A thoroughly optimized oxidation process is described in details elsewhere (Gupta *et al.*, 2009). Oxide thickness of sample was recorded using ellipsometer followed by the surface profiler verification. In order to fabricate the MOSiC structure, oxide layer from the C-face (n^+ side) of 4H-SiC was removed using buffer oxide etchant by protecting the Si-face with photoresist. Ohmic contact has been performed on the C-face with the deposition of composite layer of Ti (300 Å) and Au (2,000 Å) using e-Beam evaporation method in the vacuum range of 10^{-7} torr. The Si-face of oxidized 4H-SiC was retained with the grown oxide. A thickness of 1,500 Å of Nickel was selectively deposited on samples using e-Beam evaporation in ultra high vacuum. A metal mask carrying the array of 1.0 mm diameter was employed for the selective deposition of metal on oxide. Individual chips of MOSiC structure were separated and bonded on TO-8 header using West Bond's ball to wedge bonder. HP 4140B pA meter/ DC voltage source was used for I-V measurement while 4,284 A LCR meter m/s agilent technology was used for C-V measurement on LabVIEW-based in-house developed computer aided measurement set up. Forward I-V measurement was performed by sweeping the DC bias from 0 to 5 V with 0.1 V step voltage while for reverse I-V measurement, the voltage has been swiped from 0 to -50 V. The measurement frequency and signal level for C-V characteristics were fixed at 1 MHz and 1.0 V in case of high frequency, while 1 kHz and 1.0 V in case of low frequency, respectively. The whole C-V measurements were performed by sweeping the DC bias from -15 to 15 V with 0.2 V step voltage.

3. Experimental results and discussion

3.1 Analysis of I-V characteristics

Figure 1 shows the typical I-V characteristics of fabricated MOSiC structures for oxide thickness variation of 17.0-56.6 nm. The forward and reverse leakage current of these structures shows an asymmetric behavior with the polarity of gate bias (+ V or − V at the anode), yielding a forward leakage current density variation of 720 mA/cm^2 to 8.38 mA/cm^2 at 3.62 MV/cm and reverse leakage current density of 16 mA/cm^2 to 98 nA/cm^2 at − 72.5 MV/cm for oxide thickness range of 17 to 56.6 nm. Ideally, an oxide layer does not allow the charge carrier to pass through but practically, some amount of current always flows under the influence of electric field across the oxide layers. The life time of particular gate oxide can be determined by the total amount of charge carriers that flow through the gate oxide under the influence of external electric field. There are mainly four current conduction models (Direct tunneling, Fowler-Nordheim (F-N) tunneling, Schottky-emission, and Poole-Frenkel conduction) are available to describe the accurate conduction behavior based on the electrode limited or bulk limited phenomenon in MOS types of structures. It has been previously reported that for the oxide thickness greater than 5 nm (Lenzlinger and Snow, 1969) up to 50 nm (Zhou *et al.*, 2005) current conduction is explained by Fowler-Nordheim tunneling and in the same sequence, oxide thickness greater 50 nm is explained by Schottky emission (Zhou *et al.*, 2005). If the oxide thickness is greater than 50 nm, oxide trapped charge will affect the electrical behavior, so the current conduction mechanism will be governed by Poole-Frenkel conduction model. On the other hand, for the ultra thin oxide layers (less than 5 nm), band to band tunneling will be taken place and current conduction mechanism has been termed as direct tunneling (Maserjian, 1974). Based on our previous experimental results it has been observed that for oxide thickness range (17-56.6 nm) in MOSiC structure, current conduction mechanism is governed by F-N tunneling. In this work F-N tunneling has been used as a tool to extract barrier height at SiO_2/4H-SiC interface and temperature induced variations in the barrier heights has been systematic established and presented here.

Figure 1 Experimental current-voltage characteristics of MOSiC structure for different oxide thickness



The experimental data are fitted by F-N tunneling equation which is expressed as:

$$\mathcal{J} = AE_{\text{diel}}^2 \exp\left(-\frac{B}{E_{\text{diel}}}\right) \quad (1)$$

where J is current density, E is the oxide field, and pre-exponent A and slope B are given by:

$$A = \frac{q^3 m_{eff}}{8\pi m_{diel} h q \Phi_B} \quad (2)$$

$$= 1.54 \times 10^{-6} \frac{m_{\text{eff}}}{m_{\text{diel}}} \frac{1}{\phi_B} \left(A/V^2\right) \quad (3)$$

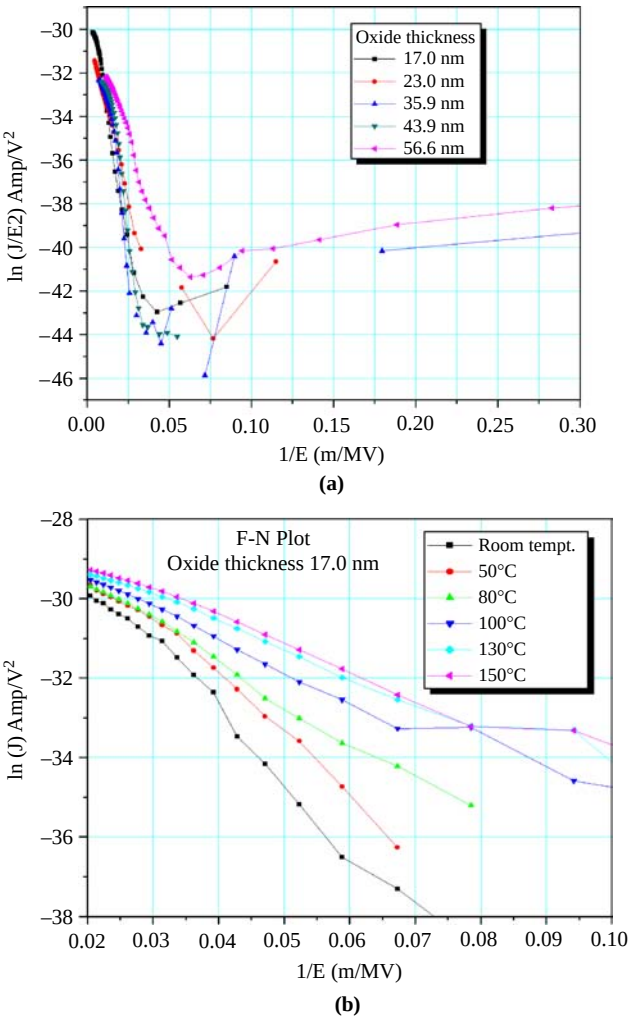
$$B = \frac{4\sqrt{2m_{diel}(q\Phi_B)^3}}{3\hbar q} \quad (4)$$

$$= 6.83 \times 10^7 \left(\frac{m_{diel}}{m_{eff}}\right)^{1/2} \phi_B^{3/2} (V/cm) \quad (5)$$

where q is the electronic charge, m_{eff} is the free electron mass in SiC, m_{diel} is the electron mass in the oxide, $\hbar$ is reduced Planck's constant and ϕ_B is barrier height at SiO_2/SiC interface.

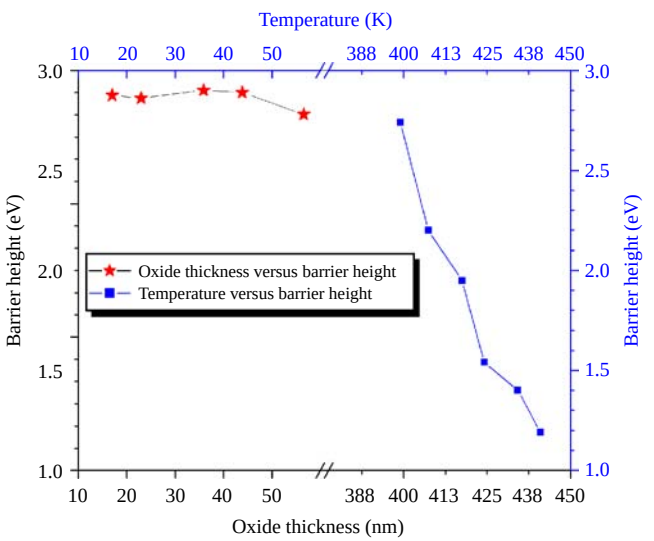
Figure 2(a) shows a linear plot of ln (J/E^2) versus 1/E called F-N plot on 4H-SiC based MOSiC structure at room temperature employing forward I-V characteristics of Figure 1. The slope of etch individual curve, i.e. for all oxide thickness had almost same value (B ~ 64 mV/cm). Using this slope, and electron effective mass in the thermal oxide of $0.55m_{\text{eff}}$ (Chanana *et al.*, 2000), the effective barrier height from 4H-SiC conduction band to the oxide conduction band has been calculated using equation (5). The value of B and electron effective mass in the thermal oxide of $0.55m_{\text{eff}}$ (Chanana *et al.*, 2000) has been putted in equation (5), gives ϕ_B of 2.80 eV. Adding the 4H-SiC band gap of 3.26 eV to the above calculated barrier height confirms the band offset determine by Afanas'ev *et al.* (1996) to be about 6 eV from the oxide conduction band to the top of the valence band in 4H-SiC. Figure 2(b) shows six straight line F-N plots of 4H-SiC based MOSiC structure having oxide thickness 17 nm at temperature ranging from room temperature up to 150°C. In same manner rest of the MOSiC structures have been plotted (results are not presented here). As the temperature increases the measured slopes decrease. In addition, the current density, at a given electric field, increases significantly with temperature. Figure 3 shows a plot of the linearly decreasing barrier height with temperature using F-N analysis. In the extraction of barrier height produced by F-N tunneling at SiO_2/4H-SiC interface, it is assumed that emitting electrode is a metal and there fore the energy distribution of tunneling electron is highly symmetric about the Fermi energy of silicon carbide. In case of n-type 4H-SiC Fermi energy is very close to the conduction band edge implying that the F-N analysis overestimates the accessibility of tunneling electrons. As temperature increases availability of conduction electron increases as the result of this F-N analysis predict larger current and correspondingly smaller effective barrier height. Increments in oxide thickness revealed the thickness increment in oxide potential width in MOSiC band diagram, while the barrier height at SiO_2/4H-SiC is unaltered (Figure 3).

Figure 2



Notes: (a) F-N plots for n-type 4H-SiC based-MOSiC structure obtained from forward I-V measurement; (b) temperature dependent F-N plots for the oxide thickness 17 nm

Figure 3 Thickness and temperature dependence barrier height at SiO_2/4H-SiC interface across MOSiC structure



3.2 Analysis of C-V characteristics

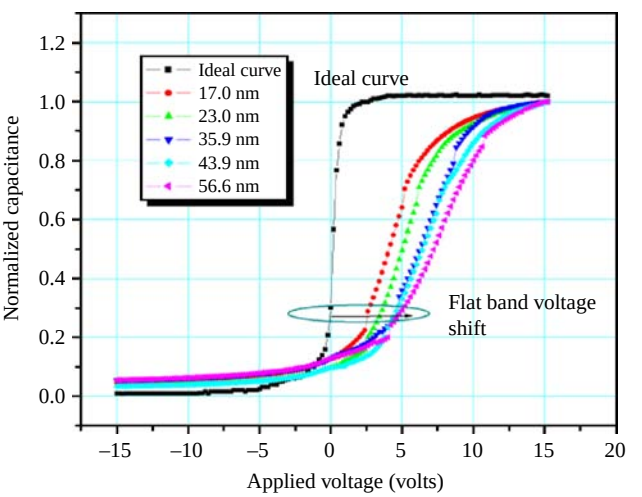
Figure 4 shows experimentally measured high frequency (H-F) C-V curve, across above explained samples (n-type MOSiC structures). The accumulation, depletion and inversion capacitance in C-V curve has been accommodated by the virtue of sweeping the voltage from − 15 to 15V. As the gate voltage is swept from accumulation to inversion or vice versa, the total oxide charge is given by:

$$Q_G = (Q_s + Q_{it}) \tag{6}$$

where Q_s is the silicon carbide charge density and Q_{it} is interface trap density. In accord to the ideal case, the interface traps (Q_{it}) should be zero means the relationship of surface potential to the gate voltage having interface traps zero is termed as an ideal C-V curve as shown in Figure 4 (square shape). When the charge is located at the oxide SiC interface, the effect of oxide charges on flatband voltage will be highest because during the sweep mode all charges will contribute in the semiconductor region. When the charge is located at the gate-oxide interface, the effective charge will contribute their presence in the gate oxide and has no effect on the flatband voltage. For a given charge density, the flatband voltage is reduced as the oxide capacitance increases, i.e. for thinner oxides. Hence, oxide charges usually contribute little to flatband or threshold voltage shifts for thin-oxide MOSiC based devices. In this work dielectric constant value of SiO_2 (3.9) is assumed to be constant for all oxide thickness. The only variable is the thickness of SiO_2. The increment in the oxide thickness might eventually decrease the total capacitance of MOSiC structures is being observed in the accumulation level of C-V curve (Figure 4). The flatband voltage shift from the ideal curve is caused by both electron or holes trapped at the interface states and in the bulk of thermally grown oxide during oxidation. To determine the various charges, one compares theoretical and experimentally measured H-F and L-F capacitance-voltage curves.

From Figure 4, a positive flatband voltage shift (ΔV_{FB}) has been observed for all of the oxides. These positive voltage shifts clearly indicate the presence of negative oxide charge in the oxide. It is believed that these negatively charged electrons have been injected from gate metal to oxide with the bias voltage. The value of fixed charge density can be computed by (Schroder, 2006):

Figure 4 Capacitance-voltage characteristics of MOSiC structure compared with ideal curve



$$Q_{fix} = \frac{1}{q}(\phi_{ms} - V_{FB})C_{ox} \quad (7)$$

where q is the electronic charge, ϕ_{ms} is the work function difference between metal and silicon carbide, V_{FB} is the flatband voltage shift and C_{ox} is the oxide capacitance. Figure 5 shows the calculated flatband voltage shift (ΔV_{FB}) as a function of oxide thickness, revealed a linear increment in ΔV_{FB} with thickness. The value of ϕ_{ms} has been determined by rewriting the equation (7) as:

$$V_{FB} = \phi_{ms} - \frac{Q_{fix}}{C_{ox}} \quad (8)$$

$$\phi_{ms} - \frac{Q_{fix}t_{ox}}{K_{ox}\varepsilon_0} \quad (9)$$

where t_{ox} is the oxide thickness K_{ox} is the dielectric constant of oxide ε_0 is permittivity of the medium. A plot of V_{FB} versus oxide thickness has a slope of $-Q_{fix}/K_{ox}\varepsilon_0$ and from the intercept on the *Y*-axis (V_{FB} axis), the exact value of ϕ_{ms} can be determined directly.

The oxide charge which is being trapped during thermal oxidation is known as oxide trapped charge, which can be determined by (Schroder, 2006):

$$Q_{oxt} = -\frac{1}{q}C_{ox}\Delta V_{FB} \quad (10)$$

where Q_{oxt} is the oxide trapped charge, C_{ox} is oxide capacitance and ΔV_{FB} is shift in flatband voltage. The trap charge may be resulting from avalanche injection, F-N tunneling or due to the formation of hot electron during device operation. Figure 6 shows the variation of oxide trap charge as a function of oxide thickness.

In the calculation of interface state density at SiO_2/4H-SiC interface a number of methods can be used. Cooper (1997) has compared different techniques and finally concluded the advantage and disadvantages of each method. In this work interface trap density (D_{it}) at the conduction band edge (E_V) of 4H-SiC was estimated from combined high and low frequency C-V measurement (Terman method) at room temperature. The details of measurement methodology have been presented

Figure 5 Variation of flat band voltage as a function of thickness

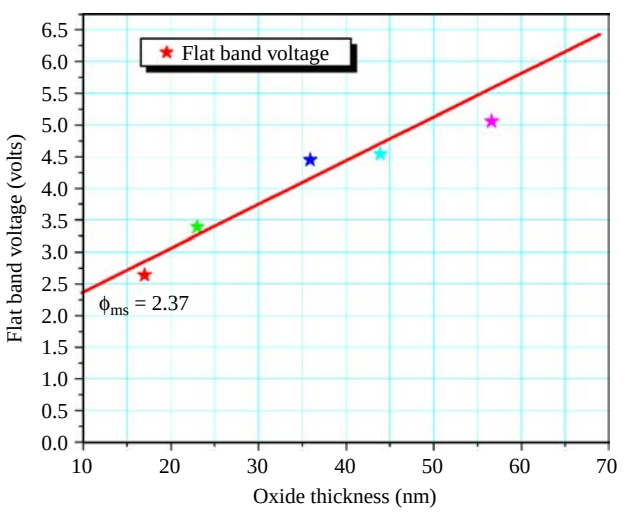
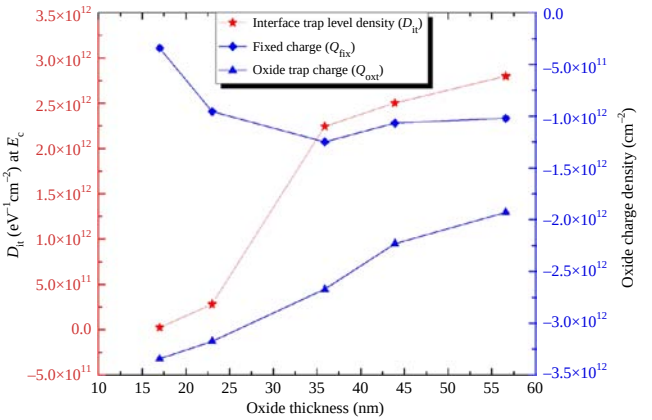


Figure 6 Different type of oxide charge variation as a function of oxide thickness



in experimental detail section of this paper. The value of D_{it} could be calculated by the following equation:

$$D_{it} = \frac{C_{ox}}{q}\left(\frac{C_{LF}/C_{ox}}{1 - C_{LF}/C_{ox}} - \frac{C_{HF}/C_{ox}}{1 - C_{HF}/C_{ox}}\right) \quad (11)$$

where, C_{LF} and C_{HF} represent the low-frequency and high-frequency capacitance, respectively. Other symbols in the above equations have their usual meaning.

A strong dependence of oxide thickness, on extracted oxide charges (Q_{fix}, Q_{oxt}, and D_{it}) has been observed. A large number of samples have been studied and all experiments have been repeated several times to confirm the results obtained in Figures 4-6. For the measured flatband voltage shift and known oxide capacitance, negative fixed charge densities were estimated, which varies from -3.42×10^{11} to -1.02×10^{12} with oxide thickness range (17.0-56.6 nm). A parabolic trend has been observed in case of fixed charge density variation as a function of oxide thickness. Deep acceptor-type interface states appear, and in this case negative fix charges are caused by both real negative fixed charges and electron captured at the deep acceptor type interface states. The increment in the positive flatband voltage shift with oxide thickness is considered to be caused by the increment of negatively charged electron during the process. During the initial growth of silicon dioxide, carbon is probable accumulated at SiO_2/4H-SiC interface (which can be shown in increasing trend in D_{it}) and caused a fixed oxide charge. When oxide thickness increases, the accumulated carbon-oxides in the bulk of grown SiO_2 will be increased because for long oxidation time (towards thicker oxide) trapping of carbon-oxide will be increased. However, this increment has a limitation. As oxide thickness increases further, increment in the bulk resistance of oxide will not allow further increment in the fixed charge, as the result distribution will become constant and the nature of the curve was seemed to be parabolic. In the extraction of Q_{oxt} for MOSiC structures, however, maximum effective trapped charge density decreases linearly having negative magnitude as oxide thickness increases. Figure 6 shows the variation of Q_{oxt} with oxide thickness. The basic reason behind this phenomenon is that the maximum effective trapped charge density in n-type MOSiC structures are limited by acceptors traps falling below the Fermi level are negatively charged. These results can be

also explained in terms of generation of acceptor traps in the upper half of the band gap. The energy distribution of the D_{it} was estimated by using equation (1), which is plotted as a function of oxide thickness (Figure 6). A continuous increment of D_{it} at the edge of the conduction band of 4H-SiC as a function of oxide thickness has been observed. It is previously reported that the interface states which distribute near the conduction band edge have a harmful influence on the channel mobility in the fabrication metal oxide semiconductor field effect transistors (Yano *et al.*, 2001). At the edge of conduction band D_{it} has been found in the range of 2.46×10^{10} to 2.80×10^{12} $cm^{-2}eV^{-1}$ by increasing the oxide thickness 17-56.6 nm (Table I). The possible origins of interface traps such as C clusters present in the bulk of oxide, dangling bonds between Si and/or C, and $Si_xC_yO_z$ are supposed to make a chemical reaction with oxidizing environment resulting in the strong addition of D_{it} near the conduction band edge of 4H-SiC. A number of methods have been adopted to reduce D_{it}. The most often process used to reduce D_{it} is post metallization annealing (Campi *et al.*, 1999), annealed in N_2O (Keiko *et al.*, 2005) or NO (Li *et al.*, 2000), thermal oxidation process modification by growth of N_2O-nitrided SiO_2 (Xu *et al.*, 2003), Sodium enhanced oxidation (Allerstam *et al.*, 2007), rapid thermal annealing (Cheong *et al.*, 2006) and so on. Oxide charges and interface trap density can be further improved or reduced by incorporating the above experimental method.

4. Conclusions

In this experiment 4H-SiC based MOSiC structure having thermally grown silicon dioxide variation of 17-56.6 nm has been fabricated and electrically characterized using, I-V and C-V techniques in order to determine the quality of thin oxide (in terms of MOS parameters) for microelectronic device application. It has been observed that current conduction mechanism is governed by F-N tunneling and extracted barrier height is independent of oxide thickness while a strong dependency has been observed under the influence of temperature. A parabolic trend has been observed in the variation of fixed oxide charge while oxide trapped charge, decreases continuously as oxide thickness increases. A linear increment in interface trap level densities as a function of oxide thickness have been also observed and reported in this paper. Electrical characterization by I-V technique and C-V techniques reveals that the low leakage current and reasonable surface states.

Table I Oxide thickness dependence of various parameter determined from I-V and C-V characteristics of MOSiC structure

Oxide thickness (nm)	Flatband voltage (V)	Barrier height (eV)	Fixed charge density (Q_{fix})	Trapped charge density (Q_{oxt}) (cm^{-2})	Interface trap level density (D_{it}) at E_C ($cm^{-2}eV^{-1}$)
17.0	2.64	2.81	-3.42×10^{11}	-3.34×10^{12}	2.46×10^{10}
23.0	3.39	2.79	-9.57×10^{11}	-3.17×10^{12}	2.80×10^{11}
35.9	4.45	2.85	-1.25×10^{12}	-2.67×10^{12}	2.25×10^{12}
43.9	4.54	2.83	-1.07×10^{12}	-2.23×10^{12}	2.50×10^{12}
56.6	5.06	2.67	-1.02×10^{12}	-1.93×10^{12}	2.80×10^{12}

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